2. (amended) The read/write amplifier as claimed in claim 1, wherein the amplifier components have at least one N latch circuit for amplifying a voltage signal to a low level and/or at least one P latch circuit for amplifying a voltage signal to a high level and/or at least one equalizer for producing a reference voltage value on the bit line(s) and the reference bit line(s) and/or at least one bit switch for connecting at least one selected bit line pair to at least one external data line.

3. (amended) The read/write amplifier as claimed in claim 2, wherein at least one N latch circuit and at least one P latch circuit are provided in the first read/write amplifier element.

4. (amended) The read/write amplifier as claimed in claim 2, wherein at least one equalizer is provided in the first read/write amplifier element.

5. (amended) The read/write amplifier as claimed in claim 2, wherein at least one N latch circuit is provided in the second read/write amplifier element.

6. (amended) The read/write amplifier as claimed in claim 2, wherein at least one bit switch is provided in the second read/write amplifier element.

7. (amended) The read/write amplifier as claimed in claim 1, wherein the second read/write amplifier element is connected or can be connected to at least one external data line.

8. (amended) The read/write amplifier as claimed in claim 1, wherein the second read/write amplifier element is connected or can be connected to at least one further read/write amplifier.

9. (amended) The read/write amplifier as claimed in claim 1, wherein the first and/or second read/write amplifier element(s) has/have one or more transistors for changing over between different bit lines and reference bit lines, respectively.

10. (amended) A DRAM memory, having a number of DRAM memory cells, which each form one or more memory cell arrays, each memory cell being connected to a bit line and the bit lines furthermore being connected to at least one read/write amplifier, wherein the at least one read/write amplifier is designed as a read/write amplifier as claimed in claim 1.

11. (amended) The DRAM memory as claimed in claim 10, wherein at least one word line is provided, which is routed across the memory cell array(s) and, for activation of the DRAM memory cells, is connected to one or more memory cell(s).

12. (amended) The DRAM memory as claimed in claim 10, wherein a plurality of bit lines of a memory cell array are connected to a read/write amplifier.

13. (amended) The DRAM memory as claimed in claim 10, wherein in each case a bit line of a DRAM memory cell that is to be evaluated and a reference bit line of a DRAM memory cell that is not to be evaluated form a bit line pair, and in that each bit line pair is connected both to the first and to the second read/write amplifier element.

14. (amended) The DRAM memory as claimed in claim 10, wherein the connection of a bit line and/or reference bit line to a read/write amplifier is activated or can be activated via one or more transistors.

15. (amended) A method for evaluating DRAM memory cells of a DRAM memory, in particular of a DRAM memory as claimed in claim 10, and in particular using a read/write amplifier as claimed in claim 1, having the following steps:

a) activation of one or more memory cells that are to be evaluated via at least one word line;

b) activation of a connection of at least one first bit line pair, formed from a bit line of the memory cell that is to be evaluated and a reference bit line of a memory cell that is not to be evaluated, to a first read/write amplifier element, and activation of the connection of at least one second bit line pair, adjacent to the first bit line pair, to a second read/write amplifier element, the two bit line pairs in each case being connected to the first and second read/write amplifier elements;

c) amplification of the voltage signals read out via the first bit line pair by means of at least one N latch circuit provided in the first read/write amplifier element and also a P latch circuit, and amplification of the voltage signals read out via the second bit line pair by means of at least one N latch circuit provided in the second read/write amplifier element;

d) evaluation and writing back of the data of the memory cell(s) that is/are to be evaluated and is/are actively connected to the first read/write amplifier element;

e) changeover of the connection between the bit line pairs and the first read/write amplifier element in such a way that the P latch circuit of the first read/write amplifier element is changed over to the second read/write amplifier element;

f) evaluation and writing back of the data of the memory cell(s) that is/are to be evaluated and is/are actively connected to the second read/write amplifier element; and

g) deactivation of the memory cells that are to be evaluated.

17. (amended) The method as claimed in claim 15, wherein the bit line pair which is actively connected to the first read/write amplifier element is disconnected from the first

read/write amplifier element after the end of step d), with the result that the bit line and the reference bit line float with full voltage levels, and in that the N latch circuit of the first read/write amplifier element is subsequently switched off.

18. (amended) The method as claimed in claim 15, wherein, after the activation of a bit switch provided in the second read/write amplifier element, a voltage difference is generated on one or more external data line(s) connected to said bit switch.

19. (amended) The method as claimed in claim 15, wherein, after the end of the evaluation operation, the uniform reference voltage is applied to all the bit lines of the evaluated memory cells via an equalizer.